UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,185	12/05/2001	Colin D. Nayler	95-525	3474

20736 7590 04/27/2006

MANELLI DENISON & SELTER
2000 M STREET NW SUITE 700
WASHINGTON, DC 20036-3307

EXAMINER	
TORRES, JUAN A	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 04/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/002,185
Filing Date: December 05, 2001
Appellant(s): NAYLER, COLIN D.

Leon R. Turkevich
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 02/07/2006 appealing from the Office action mailed 09/26/2005

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6097767	LO	8-2000

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Lo (US 6097767).

As per claim 1 Lo discloses a method in a physical layer transceiver coupled to a prescribed network medium having an undetermined length, the method comprising: supplying a prescribed initial set of equalizer settings to a digital feedforward equalizer, the digital feedforward equalizer configured for outputting equalized signal samples based on equalizing received signal samples, having encountered inter-symbol interference by transmission via the prescribed network medium, according to supplied equalizer settings (figure 1 column 2 lines 45-47); comparing the equalized signal samples relative to a prescribed equalization threshold (figure 2 column 6 lines 1-4); and selectively changing the supplied equalizer settings, based on the comparing step, until the equalized signal samples reach the prescribed equalization threshold (column 7 lines 28-41. The threshold will be the setting that causes the minimum amount of jitter in the phase locked loop. The setting that is above, or equal to this threshold is selected, because this setting provides the best performance of the equalizer).

As per claim 2 Lo discloses claim 1. Lo also discloses supplying the prescribed initial set of equalizer settings based on a predetermined characterization of the

prescribed network medium at a prescribed length (figure 1 column lines 34-39 and figure 5 column 5 lines 23-27).

As per claim 3 Lo discloses claim 2. Lo also discloses selectively changing step includes successively supplying groups of equalizer settings based on the predetermined characterizations of the prescribed network medium at successively changing lengths (figure 2 column 1 lines 34-39 and column 7 lines 28-40).

As per claim 4 Lo discloses claim 3. Lo also disclose selectively changing step includes successively generating a count interval representing reception of a statistically-based prescribed number of signal samples (column 6 lines 21-24); first determining, within the count interval, a first number of the equalized signal samples having an absolute value that exceeds a first reference level occurs for an equalized signal (column 6 lines 24-43); and second determining whether the first number reaches the prescribed equalization threshold, the prescribed equalization threshold representing an expected number of detected signal samples that exceed the first reference level within the count interval (column 6 lines 44-57. The threshold will be the setting that causes the minimum amount of jitter in the phase locked loop. The setting that is above, or equal to this threshold is selected, because this setting provides the best performance of the equalizer).

As per claim 5 Lo discloses claim 1. Lo also disclose selectively changing step includes successively generating a count interval representing reception of a statistically-based prescribed number of signal samples (column 6 lines 21-24); first determining, within the count interval, a first number of the equalized signal samples

having an absolute value that exceeds a first reference level occurs for an equalized signal (column 6 lines 24-43); and second determining whether the first number reaches the prescribed equalization threshold, the prescribed equalization threshold representing an expected number of detected signal samples that exceed the first reference level within the count interval (column 6 lines 44-57. The threshold will be the setting that causes the minimum amount of jitter in the phase locked loop. The setting that is above, or equal to this threshold is selected, because this setting provides the best performance of the equalizer).

As per claim 6 Lo discloses a physical layer transceiver configured for retrieving signal samples from a prescribed network medium having an undetermined length, the physical layer transceiver comprising: a digital feedforward equalizer configured for generating equalized signal samples from the retrieved signal samples and based on supplied equalizer settings, the retrieved signal samples having encountered intersymbol interference by transmission via the prescribed network medium (figures 1 and 2 blocks 16 and 32 column 1 line 23-32 and column); and an equalizer controller configured for supplying the supplied equalizer settings to the digital feedforward equalizer, the equalizer controller configured for supplying a prescribed initial set of equalizer settlings and comparing the equalized signal samples, having been generated based on the initial set of equalizer settings, relative to a prescribed equalization threshold, the equalizer controller configured for selectively changing the supplied equalizer settings until the equalized signal samples reach the prescribed equalization threshold (figure 2 block 36 column 4 lines 61-64. The threshold will be the setting that

causes the minimum amount of jitter in the phase locked loop. The setting that is above, or equal to this threshold is selected, because this setting provides the best performance of the equalizer).

As per claim 7 Lo discloses claim 6. Lo also discloses that the equalizer controller includes a coefficients generator configured for outputting the prescribed initial set of equalizer settings and the selectively changed equalizer settings based on a predetermined characterization of the prescribed network medium at respective prescribed lengths (figure 1 column lines 34-39 and figure 5 column 5 lines 23-27).

As per claim 8 Lo discloses claim 7. Lo also discloses that the equalizer controller further comprises a controller state machine configured for asserting an initial signal at initialization of the digital feedforward equalizer and a change signal based on a comparison result between the equalized signal samples and the prescribed equalization threshold, the coefficients generator configured for outputting a corresponding group of equalizer settings representing a successively changing network medium length in response to each corresponding assertion of the change signal (figure 5 column 5 lines 23-27 and column 7 lines 28-40).

As per claim 9 Lo discloses claim 8. Lo also discloses that the equalizer controller further comprises: a timer configured for generating a count interval representing reception of a statistically-based prescribed number of signal samples (figure 5 block 74 column 6 lines 5-12); a counter configured for determining, within the count interval, a first number of the equalized signal samples having an absolute value that exceeds a first reference level occurs for an equalized signal (figure 5 block 76

column 6 lines 24-32); and a comparator configured for outputting an equalization status signal based on whether the first number reaches the prescribed equalization threshold, the prescribed equalization threshold representing an expected number of detected signal samples that have an absolute value exceeding the first reference level within the count interval, the controller state machine selectively asserting the change signal based on the equalization status signal (figure 5 block 78 column 6 lines 44-57. The threshold will be the setting that causes the minimum amount of jitter in the phase locked loop. The setting that is above, or equal to this threshold is selected, because this setting provides the best performance of the equalizer).

As per claim 10 Lo discloses claim 1. Lo also discloses that the prescribed equalization threshold represents an expected number of detected signal samples having been detected within a prescribed count interval and having an absolute value exceeding a reference level (column 6 lines 24-43. The threshold will be the setting that causes the minimum amount of jitter in the phase locked loop. The setting that is above, or equal to this threshold is selected, because this setting provides the best performance of the equalizer).

As per claim 11 Lo discloses claim 10. Lo also discloses that the reference level identifies a prescribed minimum value necessary for an ideal equalized signal sample to be detected as a prescribed data value (column 6 lines 44-57)

As per claim 12 Lo discloses claim 6. Lo also discloses that the prescribed equalization threshold represents an expected number of detected signal samples having been detected within a prescribed count interval and having an absolute value

exceeding a reference level (column 6 lines 24-43. The threshold will be the setting that causes the minimum amount of jitter in the phase locked loop. The setting that is above, or equal to this threshold is selected, because this setting provides the best performance of the equalizer).

As per claim 13 Lo discloses claim 12. Lo also discloses that the reference level identifies a prescribed minimum value necessary for an ideal equalized signal sample to be detected as a prescribed data value (column 6 lines 44-57)

(10) Response to Argument

Applicant's arguments filed on 02/07/2006 have been fully considered but they are not persuasive.

Regarding claims 1 and 6:

The Applicant contends, "A1. Lo et al. Does Not Disclose or Suggest the Claimed Selectively Changing the Equalizer Settings Until the Equalized Signal Samples Reach the Prescribed Equalization Threshold".

The Examiner disagrees and asserts, that, as indicated in the previous Office action, Lo discloses an apparatus and method for determining an optimum equalizer setting for a signal equalizer in a communication network receiver (title of the patent); and an optimum equalizer setting is determined for a signal equalizer in a network receiver by successively setting the equalizer to different predetermined settings (abstract).

Lo discloses:

"An optimum equalizer setting is determined for a signal equalizer in a network receiver by successively setting the equalizer to different predetermined settings, detecting timing correlation results between the equalized signal and a recovered clock in a digital phase locked loop, and determining a normalized distribution result for each of the predetermined equalizer settings based on the timing correlation results. The equalizer setting having the minimum normalized distribution result can then be selected as the optimum equalizer setting. Use of the correlation result from the phase locked loop enables the equalizer controller determining the optimum equalizer setting to determine the setting using a closed-loop setting. Hence, the equalizer controller can effectively determine the equalizer setting that causes the minimum amount of jitter in the phase locked loop" (abstract)

"According to the disclosed embodiment, an optimum equalizer setting is determined for a signal equalizer by successively setting the equalizer to different predetermined settings, and determining the normalized distribution result for each of the predetermined equalizer settings based on timing correlation results output by the digital phase locked loop. Hence, the optimum equalizer setting can be quickly determined to minimize jitter. According to the disclosed embodiment, the entire procedure for determining the optimum equalizer setting can be executed within one millisecond of exiting the blind wait state 74. Hence, the disclosed arrangement is particularly effective for receiver systems in 100 Mb/s Ethernet (IEEE 802.3) networks" (column 7 lines 28-41);

"Another alternative involves detection of a local minimum, as shown in FIG. 6B. For example, assume that the entire domain of equalizer settings includes settings A, B, C, D, E, F, and G. If equalizer settings C, D, and E each have the same minimum outside count indicating a local minimum in state 82a, the state 82b will select the middle equalizer setting (e.g., D) as the optimum equalizer setting" (column 8 lines 20-27);

"Although the disclosed embodiment describes successively testing equalizer settings by starting with the predetermined equalizer setting corresponding to a minimum length and successively testing equalizer settings for successively longer cable lengths, the disclosed embodiment is not limited to any particular sequence for testing the equalizer settings. For example, the disclosed embodiment may be modified by initially testing the equalizer setting corresponding to the maximum length setting, and successively testing equalizer settings for successively shorter cable lengths" (column 8 lines 27-38); and

"While this invention has been described in connection with what is presently considered to be the most practical and preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims" (column 8 lines 39-45)

The Applicant contends, "A1 (i) Lo et al.'s Prior Art Receiver Does Not Disclose the Claimed Selectively Changing".

The Examiner disagrees and asserts, that, as indicated in the previous Office action, Lo discloses that an optimum equalizer setting is determined for a signal equalizer in a network receiver by successively setting the equalizer to different predetermined settings (abstract).

Lo discloses:

"An optimum equalizer setting is determined for a signal equalizer in a network receiver by successively setting the equalizer to different predetermined settings, detecting timing correlation results between the equalized signal and a recovered clock in a digital phase locked loop, and determining a normalized distribution result for each of the predetermined equalizer settings based on the timing correlation results. The equalizer setting having the minimum normalized distribution result can then be selected as the optimum equalizer setting. Use of the correlation result from the phase locked loop enables the equalizer controller determining the optimum equalizer setting to determine the setting using a closed-loop setting. Hence, the equalizer controller can effectively determine the equalizer setting that causes the minimum amount of jitter in the phase locked loop" (abstract)

The Applicant contends, "A1(ii) Lo et al.'s Equalizer 32 and Equalizer Controller 32 Do Not Disclose the Claimed Selectively Changing".

The Examiner disagrees and asserts, that, as indicated in the previous Office action, Lo discloses that an optimum equalizer setting is determined for a signal equalizer in a network receiver by successively setting the equalizer to different predetermined settings (abstract).

Lo discloses:

"An optimum equalizer setting is determined for a signal equalizer in a network receiver by successively setting the equalizer to different predetermined settings, detecting timing correlation results between the equalized signal and a recovered clock in a digital phase locked loop, and determining a normalized distribution result for each of the predetermined equalizer settings based on the timing correlation results. The equalizer setting having the minimum normalized distribution result can then be selected as the optimum equalizer setting. Use of the correlation result from the phase locked loop enables the equalizer controller determining the optimum equalizer setting to determine the setting using a closed-loop setting. Hence, the equalizer controller can effectively determine the equalizer setting that causes the minimum amount of jitter in the phase locked loop" (abstract)

The Applicant contends, A1 (iii) The Rejection Fails to identify the Claimed Selectively Changing".

The Examiner disagrees and asserts, that, as indicated in the previous Office action, Lo discloses that an optimum equalizer setting is determined for a signal equalizer in a network receiver by successively setting the equalizer to different predetermined settings (abstract).

Lo discloses:

"An optimum equalizer setting is determined for a signal equalizer in a network receiver by successively setting the equalizer to different predetermined settings, detecting timing correlation results between the equalized signal and a recovered clock

in a digital phase locked loop, and determining a normalized distribution result for each of the predetermined equalizer settings based on the timing correlation results. The equalizer setting having the minimum normalized distribution result can then be selected as the optimum equalizer setting. Use of the correlation result from the phase locked loop enables the equalizer controller determining the optimum equalizer setting to determine the setting using a closed-loop setting. Hence, the equalizer controller can effectively determine the equalizer setting that causes the minimum amount of jitter in the phase locked loop" (abstract)

The Applicant contends, "A2. Lo et al. Does Not Disclose or Suggest the Claimed Equalization Threshold".

The Examiner disagrees and asserts, that, as indicated in the previous Office action, Lo discloses that an optimum equalizer setting is determined for a signal equalizer in a network receiver by successively setting the equalizer to different predetermined settings (abstract). The threshold will be the setting that causes the minimum amount of jitter in the phase locked loop. The setting that is above, or equal to this threshold is selected, because this setting provides the best performance of the equalizer.

Lo discloses:

"An optimum equalizer setting is determined for a signal equalizer in a network receiver by successively setting the equalizer to different predetermined settings, detecting timing correlation results between the equalized signal and a recovered clock in a digital phase locked loop, and determining a normalized distribution result for each

of the predetermined equalizer settings based on the timing correlation results. The equalizer setting having the minimum normalized distribution result can then be selected as the optimum equalizer setting. Use of the correlation result from the phase locked loop enables the equalizer controller determining the optimum equalizer setting to determine the setting using a closed-loop setting. Hence, the equalizer controller can effectively determine the equalizer setting that causes the minimum amount of jitter in the phase locked loop" (abstract).

The Applicant contends, "B. Lo et al. Does Not Disclose the Claimed Prescribed Equalization Threshold of Claims 4-5, 9-13".

The Examiner disagrees and asserts, that, as indicated in the previous Office action, Lo discloses and an optimum equalizer setting is determined for a signal equalizer in a network receiver by successively setting the equalizer to different predetermined settings (abstract). The threshold will be the setting that causes the minimum amount of jitter in the phase locked loop. The setting that is above, or equal to this threshold is selected, because this setting provides the best performance of the equalizer.

Lo discloses:

"An optimum equalizer setting is determined for a signal equalizer in a network receiver by successively setting the equalizer to different predetermined settings, detecting timing correlation results between the equalized signal and a recovered clock in a digital phase locked loop, and determining a normalized distribution result for each of the predetermined equalizer settings based on the timing correlation results. The

equalizer setting having the minimum normalized distribution result can then be selected as the optimum equalizer setting. Use of the correlation result from the phase locked loop enables the equalizer controller determining the optimum equalizer setting to determine the setting using a closed-loop setting. Hence, the equalizer controller can effectively determine the equalizer setting that causes the minimum amount of jitter in the phase locked loop" (abstract).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Juan Alberto Torres

04-24-2006

Conferees:

Mohammed Ghayour

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER

Chieh Fan

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER